AN00146: Implementing a Relay Barrier with FlashRunner In-System Programmers

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1. Introduction

The aim of this application note is to help you analyze and understand how to implement an ISP signal relay barrier in your In-System Programming application.

This application note is mainly intended for FlashRunner integration as part of an Automatic Testing Equipment (ATE). However, the same considerations can be applied to any FlashRunner installation as part of a dedicated programming station.

In most applications, the In-System Programming phase is preceded and followed by a testing phases.

Before the programming phase, a parametric test can be performed—in this case, the test typically consists of checking the values of resistors, capacitors, etc. During this phase the board is powered off and it's important to avoid any external interference with other parts of the ATE system.

After the programming phase, a functional test can be performed in order to check for normal board functionality. During this test the board is powered on and the ATE system typically performs analog and digital measurements.

Both the parametric and functional test require that the Board Under Test (BUT) is not connected to external devices (such as an In-System Programmer). To achieve isolation from the programmer a relay barrier is required.

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2. Typical Application

The figure below shows an ATE system used to test and program an electronic board.

Figure 1. ATE with Automatic Feeder

The BUT is either held inside a specific fixture with an automatic feeder (as shown in the picture above), or inside a manual fixture (as shown in the figure below).

Figure 2. ATE with Manual Fixture

The typical operations performed by the ATE system to the BUT are:

- Parametric test
- In-System Programming
- Functional test

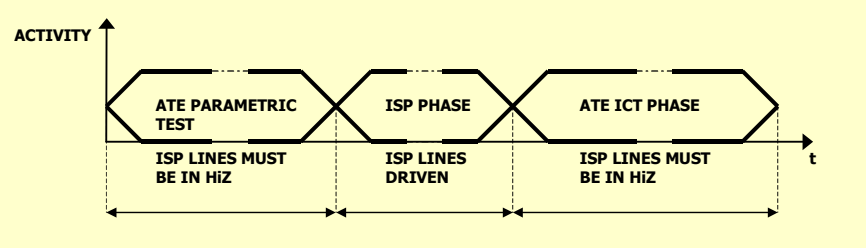

Figure 3. ATE Operations Sequence

Specific applications could require different operations in a different order. The important thing to understand is that, during the phases that do not involve programming, an In-Circuit Programmer should drive ISP lines to HiZ in order to avoid conflict with the operations that the ATE system could perform on those lines.

In particular, during the parametric test the BUT is powered off and measurement of resistors and capacitors are performed. During this test, current and voltage measurements with a precision of $10^{-6} \div 10^{-9}$ units or higher are performed. In this scenario, even a current leakage in the order of 10^{-6}A or a residual voltage in the order of 10^{-9}V provided by the programmer on ISP lines could become an issue.

Similarly, if an Automatic Optical Inspection (AOI) test is replaced by capacitance measurements (to establish, for example, the quality of soldering), the parasitic capacitance introduced by the programmer on ISP lines could become an issue.

3. FlashRunner FR01ENG, FR01PRO, FR01LAN and FR03

The technology used to drive the ISP lines to high impedance depends on the specific FlashRunner model.

FlashRunner FR01ENG, FR01PRO, FR01LAN and FR03 feature an ISP line driver for purely digital lines (DIO[6..2] and CLKOUT) as detailed in the following diagram.

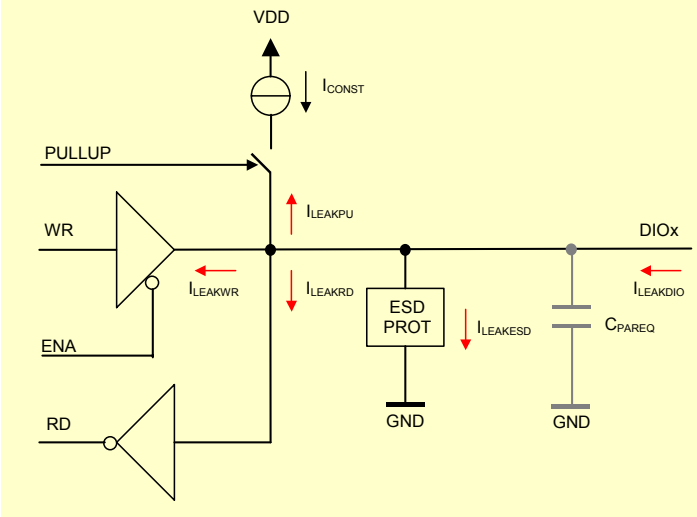

Figure 5. FlashRunner DIO[6..2] and CLKOUT Lines Stage

The leakage current on each digital ISP line is:

$$I_{LEAKDIOx} = |I_{LEAKPU}| + |I_{LEAKWR}| + |I_{LEAKRD}| + I_{LEAKESD}$$

Since each leakage current that contributes to the total leakage current could be either positive (sinking) or negative (sourcing) with respect to the chosen direction (exception made for $I_{LEAKESD}$, that is always positive), the module of these value is used, and the equivalent leakage current represents the worst case.

Using the maximum leakage current indicated in the components' datasheets, the resulting maximum leakage current is:

$$I_{LEAKDIOX} = |\pm 0.5nA| + |\pm 0.5\mu A| + |\pm 0.1\mu A| + 1\mu A = 1600.5nA \cong 1.6\mu A$$

The parasitic equivalent capacitance is:

$$C_{PAREQ} = C_{PARPU} + C_{PARWR} + C_{PARRD} + C_{PARESD} =$$
$$= 37pF + 8pF + 6pF + 9.5pF =$$
$$= 60.5pF \cong 60pF$$

The ISP stage for the analog/digital ISP lines (AO/DIO[1..0]) is shown in the following diagram.

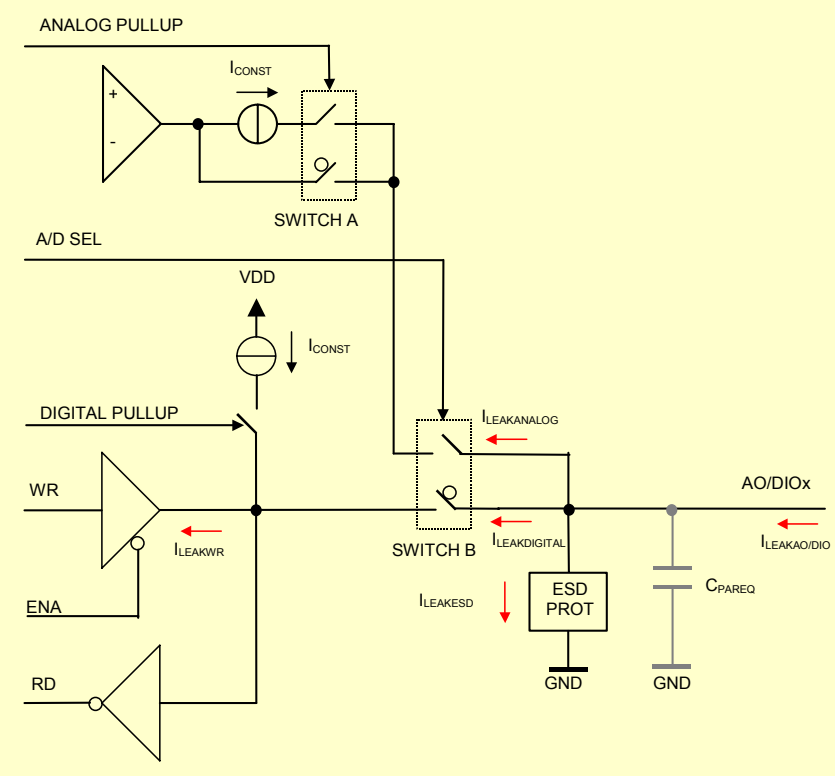

Figure 6. FlashRunner AO/DIO[1..0] Lines Stage

The leakage current on each analog/digital ISP line is:

$$I_{LEAKAO/DIO} = |I_{LEAKANALOG}| + |I_{LEAKDIGITAL}| + I_{LEAKESD}$$

As previously noted, each leakage current that contributes to the total leakage current can be either positive (sinking) or negative (sourcing). Therefore the module of these value is used, exception made for $I_{LEAKESD}$, which is always positive (sinking).

Using the maximum leakage current indicated in the components' datasheets, the resulting maximum leakage current is:

$$I_{LEAKDIO} = |\pm 0.5nA| + |\pm 0.5nA| + 2\mu A = 2001nA \cong 2\mu A$$

The parasitic equivalent capacitance at f = 1MHz is:

$$C_{PAREQ} = C_{PARANALOG} + C_{PARDIGITAL} + C_{PARESD} = 37pF + 37pF + 3pF = 77pF$$

The VPROG[1..0] programmable power lines stage (where available) is implemented as shown in the diagram below.

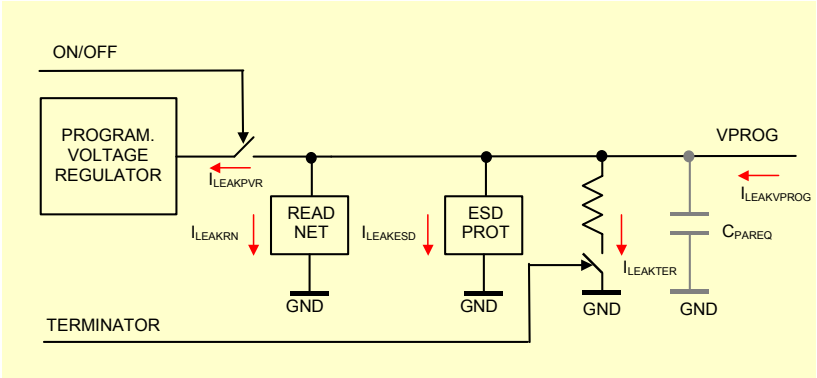

Figure 7. FlashRunner VPROG[1..0] Lines Stage

The leakage current on each programmable power ISP line is:

$I_{LEAKVPROG} = I_{LEAKPVR} + I_{LEAKRN} + I_{LEAKESD} + I_{LEAKTER}$

Using the maximum leakage current indicated in the components' datasheets, the resulting maximum leakage current (with 6V applied to VPROG[1..0]) is:

$I_{LEAKVPROG} = 0.5\mu A + 1050\mu A + 800\mu A + 0.5\mu A = 1850\mu A \cong 1.85mA$

The parasitic equivalent capacitance at f = 1MHz is:

$C_{PAREQ} = C_{PARPVR} + C_{PARRN} + C_{PARESD} + C_{PARTER} =$
$= 75pF + 3pF + 3000pF + 25pF = 3103pF \cong 3.1nF$

Conclusion

The DIO[6..2] and CLKOUT leakage current of 1.6µA, and the AO/DIO[1..0] leakage current of 2µA is of the same order of magnitude of the maximum precision requested by some in-circuit test on the BUT. Note that the equivalent parasitic capacitance, even if always lower than 100pF, could be an issue during some specific tests.

In most cases, the leakage current of VPROG[1..0] should not cause any trouble, since the accuracy requested for the measurements on BUT power lines are usually less precise. The same consideration can be applied to the equivalent parasitic capacitance.

4. FlashRunner FR01M01

FlashRunner FR01M01 implements the DIO/AO[1..0] ISP lines stage (on every ISP site) as illustrated in the diagram below.

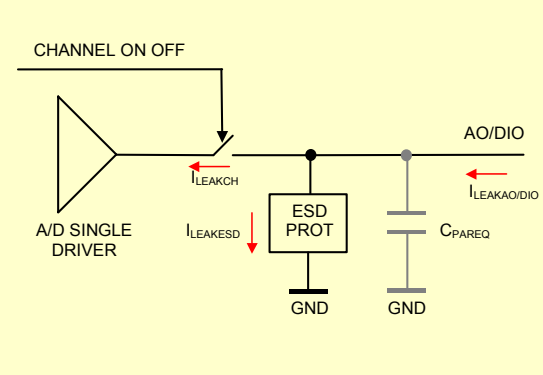

Figure 8. FR01M01 AO/DIO ISP lines stage

The leakage current on each AO/DIO ISP line is:

$I_{LEAKAO/DIO} = |I_{LEAKCH}| + I_{LEAKESD}$

Using maximum leakage currents from components' datasheets, and substituting:

$I_{LEAKAO/DIO} = |\pm 5nA| + 3nA = 7nA$

The equivalent parasitic capacitance at 3V, f = 1MHz is:

$C_{PAREQ} = C_{PARCH} + C_{PARESD} = 40pF + 0.6pF = 40.6pF \cong 40pF$

DIO[6..2] and CLKOUT lines are implemented as illustrated in the figure below.

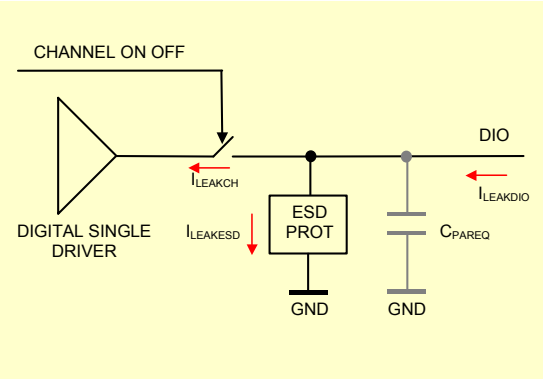

Figure 9. FR01M01 DIO[6..2] and CLKOUT ISP Lines Stage

The leakage current for each DIO ISP line is:

$I_{LEAKDIO} = |I_{LEAKCH}| + I_{LEAKESD}$

Using maximum leakage currents from components' datasheets, and substituting:

$I_{LEAKDIO} = |\pm 0.3nA| + 1\mu A = 1000.3nA \cong 1\mu A$

The equivalent parasitic capacitance at 3V, f = 1MHz is:

$C_{PAREQ} = C_{PARCH} + C_{PARESD} = 9pF + 9.5pF = 18.5pF$

VPROG[1..0] lines feature a true high impedance stage, thanks to Reed relays, as illustrated in the figure below.

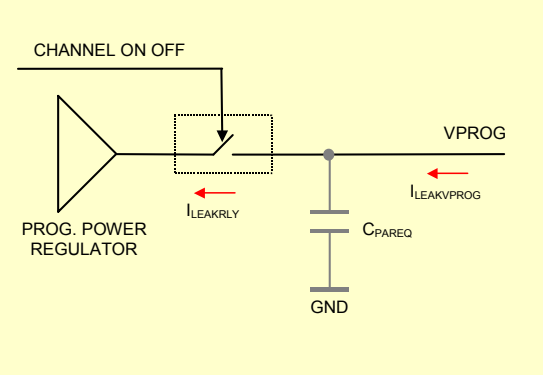

Figure 10. FR01M01 VPROG[1..0] ISP Lines Stage

The leakage current for VPROG[1..0] lines is:

$I_{LEAKDIO} = I_{LEAKRLY} = 0\ A$

The equivalent parasitic capacitance at 10KHz is:

$C_{PAREQ} = C_{PARRLY} = 0.8pF \cong 0\ F$

Conclusion

Even if lower than in other FlashRunner models, the leakage current on some FR01M01 ISP lines should not be ignored during in-circuit test on the BUT. C_{PAREQ} is also lower, but during some a highly accurate test it could be a problem.

5. FlashRunner FR01AT0

FlashRunner FR01AT0 implements the following stage for all of the ISP lines.

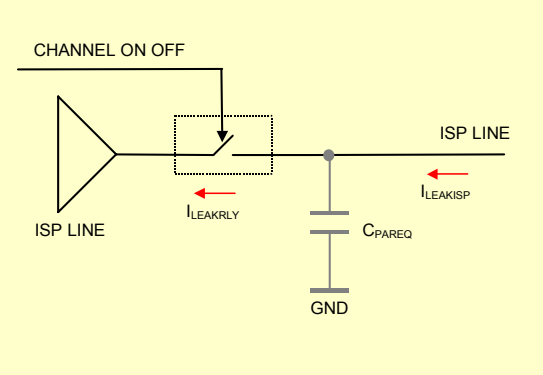

Figure 11. FR01AT0 ISP Lines Stage

$I_{LEAKISP} = I_{LEAKRLY} = 0A$

All of the ISP lines feature a Reed relay, so the equivalent leakage current is 0A. This will guarantee a non-intrusive behaviour during highly accurate BUT tests.

The equivalent parasitic capacitance for all of the IPS lines is:

$C_{PAREQ} = C_{PARRLY} = 1pF$

Conclusion

FlashRunner FR01AT0 doesn't suffer from leakage current problems, even if the in circuit tests performed on the BUT are extremely accurate. The equivalent parasitic capacitance is also low and is negligible compared to wiring parasitic capacitance.

6. FlashRunner ISP Stage Considerations

The overview of the ISP lines technology implemented in the various FlashRunner models should help you decide which model is better suited to your in-circuit tests, depending on the accuracy of your measurements. While FlashRunner FR01AT0 is the most reliable choice, the other models may need an external relays barrier in order to achieve true high impedance on ISP lines.

Don't turn FlashRunner off during in-circuit tests: the resulting low impedance on ISP lines will degrade the measurements and/or could lead to test failure.

7. Adding an External Relay Barrier

If required, an external relay barrier can be added, as shown in the figure below.

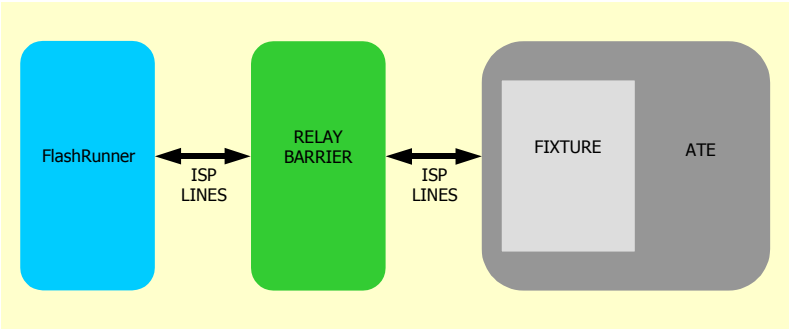

Figure 12. Adding an External Relay Barrier

Relay Barrier Placement

As a general rule, the relay barrier should be placed as near as possible to the bed of nails, in order to keep the length of the wiring between the relay barrier and the nails as short as possible—and consequently achieve the lowest parasitic capacitance. This will ensure that high-accuracy tests (like measurements of rise and fall time, frequency, etc.) can be precisely performed on ISP lines.

The relay barrier should be placed in an easily accessible area, since mechanical relays can only perform for a limited number of actuations and need to be replaced at the end of their lifetime.

A good choice for placement is therefore inside the test fixture, since most fixtures provide enough space to integrate a relay barrier.

Choosing the Right Relay Technology

Choosing the right relay technology is a key point when designing the relay barrier for your in-circuit programming application. These relays must have a low static contact resistance, in order to keep the voltage across the contacts (when the current flows through the relay) as low as possible.

In particular, the minimum voltage drop between contacts must be lower than 100-200µV; in most cases the relay manufacturer classifies this kind of relays as test and measurement relays, or relays for ATE applications.

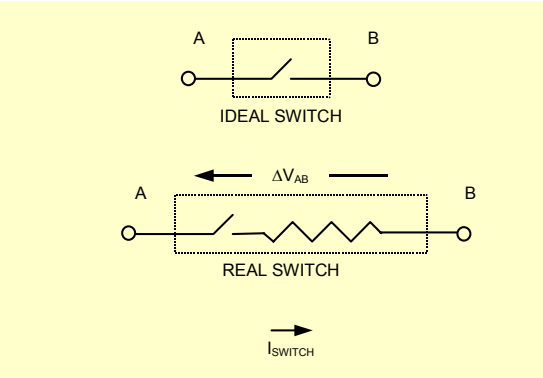

Figure 13. Relay Parasitic Resistance

The static contact resistance is important when the signal voltage swing is small. In this case, even a small resistance around 1Ω plays an important role with low currents (in the order of magnitude of few hundreds of mA). In fact, the typical voltage swing of in-system programming signals is 5V or less.

Another key element to evaluate when choosing the relay is the parasitic capacitance.

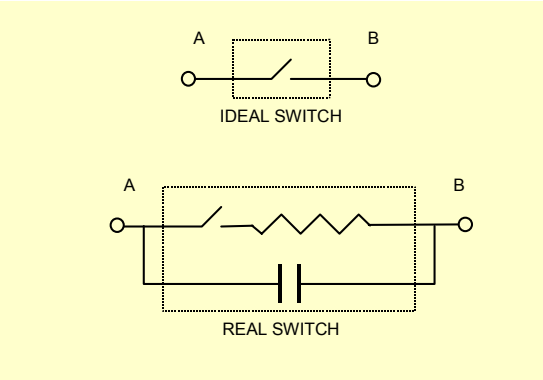

Figure 14. Relay Parasitic Capacitance

The relay manufacturers typically give the capacitance across the open contact, and the capacitance between coil and contacts. As already stated, in order to achieve accurate dynamic tests, the parasitic capacitance should be as low as possible. Relay with C_{PAR} across the contacts and between the coil and contact less than 20-30pF are suitable for this kind of application.

Carry current and switching current should be evaluated keeping in mind that the FlashRunner's ISP line which draws the most current is the VPROG0 line, drawing at most 500mA. Of course, a safe margin (at least 40%) should be applied:

$$I_{SWITCH} = I_{FLASHRUNNERmaximum} + 40\%\ I_{FLASHRUNNERmaximum}$$

Carry current and switching current greater than 0.7A are suitable.

Operating times (including bounce time at contact closing) are in most cases not important, since FlashRunner features a programmable software delay between the relay driving (closing or opening contact) and the subsequent ISP operations. Anyway, fast operating times are preferred, especially in cases where no coil suppressor circuitry is present.

Relay lifetime is not a key issue. However, the higher the relay lifetime the better. Relay manufacturers provide lifetime expressed as the number of operations/cycles at a given carry current and voltage across the contacts. Obviously, depending on your specific application, actual relay lifetime could vary by a large degree. The typical lifetime expected range for relays used in this kind of applications is from 10^6 to 10^8 operations.

Typically, the most stressed relays in the barrier are those used for the VPROG0 and VPROG1 lines, since the current drawn by these lines is greater than other ISP line's. A good design should include a relay counter to keep track of the number of operations, and advise the operator when a predefined maximum value is reached.

FlashRunner FR01M01 and FR01AT0 models feature built-in relay counters.

8. Relay Failure

Relays may fail for the following reasons:

- Relay doesn't open when the coil is released (sticking);
- Relay doesn't close when the coil is biased;
- Static on resistance across the contacts exceeds the allowed maximum.

Additionally, relay failures can be of two types: soft or hard failure, depending on whether the failure is permanent or temporary (relay sometimes misses activation). Since an ISP application requires high reliability, even occasional malfunctioning cannot be accepted. This is why correct relay barrier design and regular maintenance are of the utmost importance.

9. Driving the Relay Barrier

The relay barrier can be driven in three ways. In the first two ways, driving is directly performed by FlashRunner; in the third way, driving is performed by the ATE system.

Driving Through FlashRunner's VPROG0 or VPROG1 Power Line

In this driving mode, the relays are driven through either the VPROG0 or VPROG1 line. Wiring is shown in the figure below.

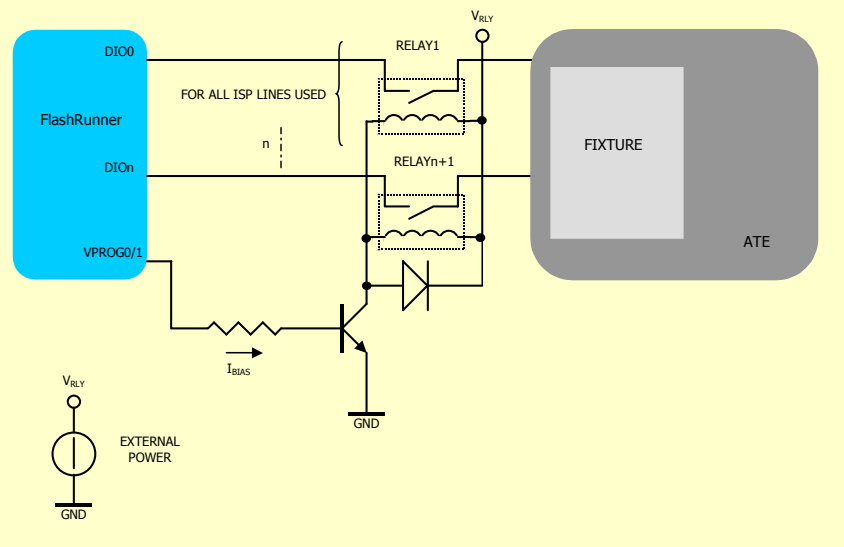

Figure 15. Relay Driving Through VPROG0 or VPROG1 Line

All of the ISP lines (including VPROG0, VPROG1 and GND) implement a relay. Basically, the relays are driven through just one or *n* NPN transistors, or any other IC dedicated to relay driving (such as a Darlington array like the ULN2803). In case of a dedicated IC, the clamp diode is usually integrated. The power for the relays is provided by an external power supply. The relay ground is common to the other ISP signals.

The total current needed by the relay barrier is:

$$I_{RELAY} = (V_{RLY} / R_{RLY}) \times n + I_{BIAS}$$

I_{BIAS} can be ignored since it's small compared to other currents.

The voltage supplied by the external power supply depends on the relays used. Typically, 5V or 12V DC coil relays are suitable for this kind of application.

The relays can be either SPST or SPDT (or DPST or DPDT). When not biased or unpowered, the contacts must be open: for this reason, in the case of a SPDT relay, the ISP line from the BUT must be connected to the N.O. relay pin.

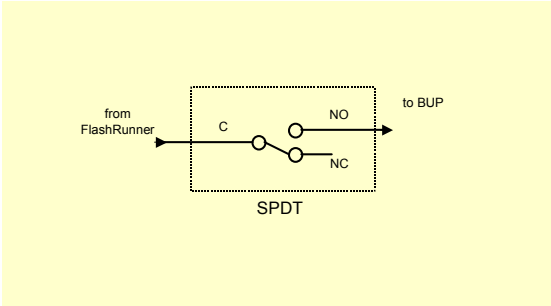

Figure 16. SPDT Relay

Also, no-latch relay versions must be used.

It's very important to use a relay even for the GND ISP line due to the fact that, under some circumstances, a ground connection acts like an antenna and could cause the in-circuit testing to fail.

Script Hints

Relay "bouncing time" is a natural phenomenon of a mechanical relay. To compensate for the relay signal bouncing when contacts close, a proper power up time must be specified in the FlashRunner script.

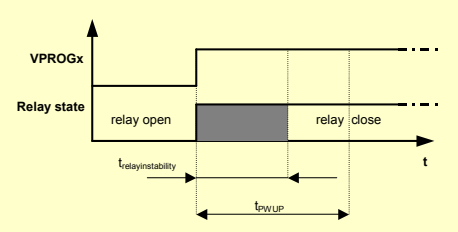

Figure 17. Relay Bouncing Time

The PWUP time must be greater than the time needed for the relay to achieve stable signal (shaded area in the picture above).

```
; Power up time (from 0 ms to 65535 ms)
; set greater than tRELAYSTABILIZATION
   TCSETPAR PWUP 50
```

Typically, Reed relays have a bouncing time (when contacts close) of 10-20ms.

No adjustment is needed for the PWDOWN time, since after the VPROGx is driven low the ISP lines stay in HiZ and no more actions are performed on BUT.

This relay control method doesn't work with Freescale HC08 and RS08 devices, since for programming these microcontrollers some ISP lines must be driven prior to driving the VPROGx lines. For these devices, please refer to the other relay driving methods.

Driving Through FlashRunner's BUSY Line

In this driving mode, the relays are driven through the BUSY control line. Wiring is shown in the figure below.

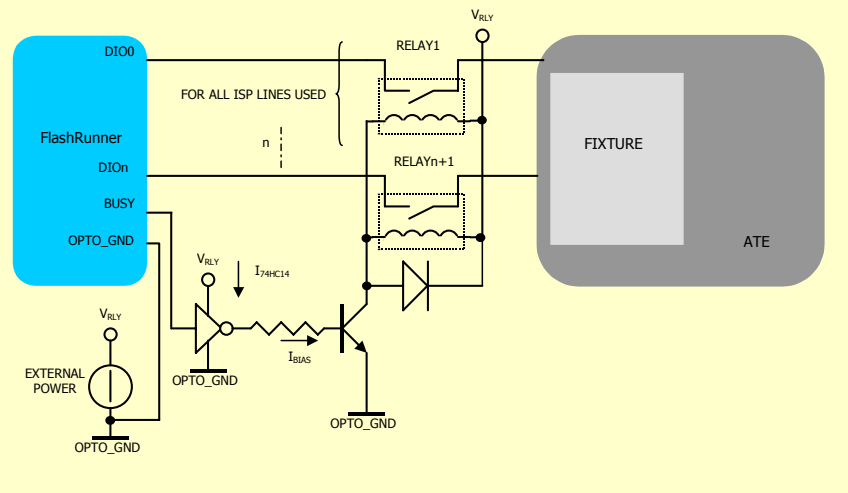

Figure 18. Relay Driving Through BUSY Line

All ISP lines are switched through a relay, including VPROG[1..0] and GND. Both a discrete NPN transistor and an IC transistor array are suitable as relay drivers. Of course, an external power supply is needed in order to power the relay coils. In this case, the ground of the external power supply must be connected to FlashRunner's OPTO_GND line, since the BUSY line is optoisolated and referenced to OPTO_GND.

Additionally, an external inverter is needed in order to invert the BUSY signal. An ordinary single-gate 74HC14 IC, or any another common-emitter transistor inverter, can be used.

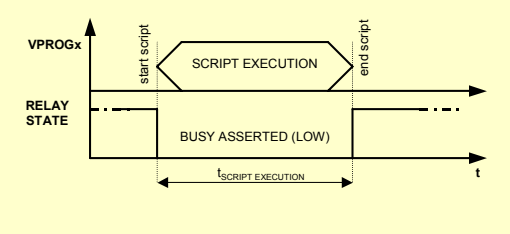

Figure 19. BUSY Line Driving

The BUSY signal is active low, and pulled through a resistor to 5V when not driven.

Regarding the type of relay to use (no latching) and the power consumption, the considerations done in the previous section ("Driving Through FlashRunner's VPROG0 or VPROG1 Power Line") are still valid. In this case, I_{BIAS} and I_{74HC14} are negligible and can be ignored.

Script Hints

To avoid problems caused by the relay signal bouncing when contacts close, the PWUP time should be set to a value greater than the bouncing time.

Driving Through ATE Lines

In this driving mode, the relays are driven through the ATE programmable lines. This relay driving mode assumes that at least one ATE general-purpose line is available and controllable before running the FlashRunner script. Wiring is shown in the figure below.

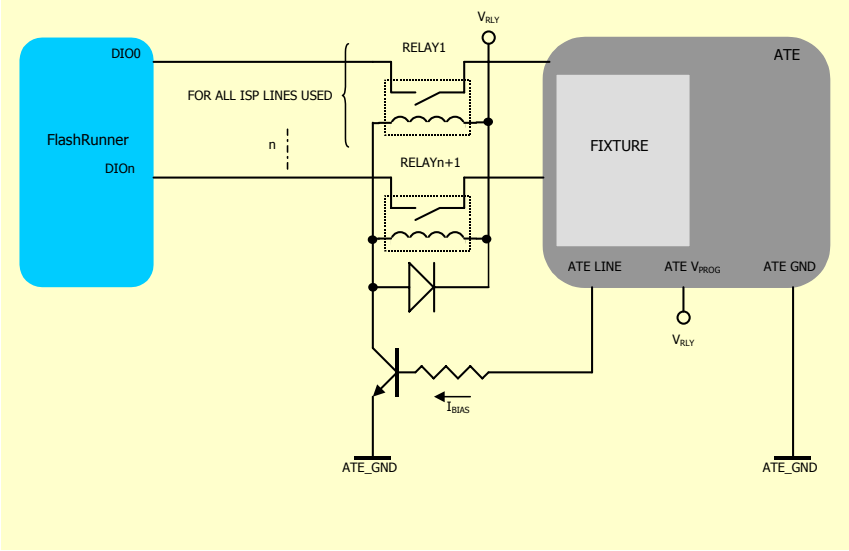

Figure 20. Relay Driving Through ATE Signals

As in the cases explained before, all of the ISP lines are switched through a relay, and the relay drivers can be either discrete or IC transistors. The relay driver (a single NPN transistor in the figure) is controlled through an ATE general purpose line. The power supply for the relay coil also comes from an ATE programmable power output; however, any external power supply can be used.

The figure shows a relay driving ground that is different from FlashRunner's ISP lines ground. However, the FlashRunner's ISP lines ground could be used instead, as long as no ground loop is created with the BUT ground—this would make the isolation function of the GND relay useless.

For power consumption, please refer to the considerations done in the previous relay driving mode discussions.

10. Conclusion

This application note has shown the design of the ISP stage of every FlashRunner model, has highlighted the parasitic effects of the different solutions implemented, and has suggested a workaround every time a true high impedance is needed in order to perform trouble-free in-system testing.

To achieve isolation from the programmer during in-system testing, a relay barrier is required. Three different relay driving methods, and relative issues, have been discussed.