AN00178: eMMC, NAND, NOR programming with FlashRunner 2.0

FlashRunner 2.0 is a Universal In-System Programmer, which uses the principles of In-Circuit Programming to program eMMC, NAND and NOR memories. This Application Note describes how to properly set up and use FlashRunner 2.0 to program devices.

This Application Note assumes that you are familiar with both FlashRunner and the main features of the eMMC, NAND and NOR memories. Full documentation about these topics is available in the FlashRunner 2.0 User's Manual and in device-specific datasheets.

1. Introduction

In-system programming of eMMC, NAND and NOR memories features can be achieved with dedicated communication protocols. Each memory type can be programmed using several data line subset defined by a particular communication protocol mode:

- eMMC: 1bit, 4bit (1 ISP channel reserved for each device), 8bit (2 ISP channels reserved for each device),

- NAND: 8bit, 16bit (4 ISP channels reserved for each device),

- NOR: 32bit (8 ISP channels reserved for each device),

This means that, at first, you need to double check on target board how many data lines are brought out through test points or connector pins. Then, you can choose your favorite communication protocol. Of course, the more data lines are connected, better performances are. On the contrary, all communication protocols which requires more than 1 ISP channel can't work mixed with other communication protocols.

This considerations drive to the following table, based on a FLASHRUNNER2.0A16 channels. Each cell reports how many devices in parallel you can program and protocols you can mix up when configuring ISP channels.
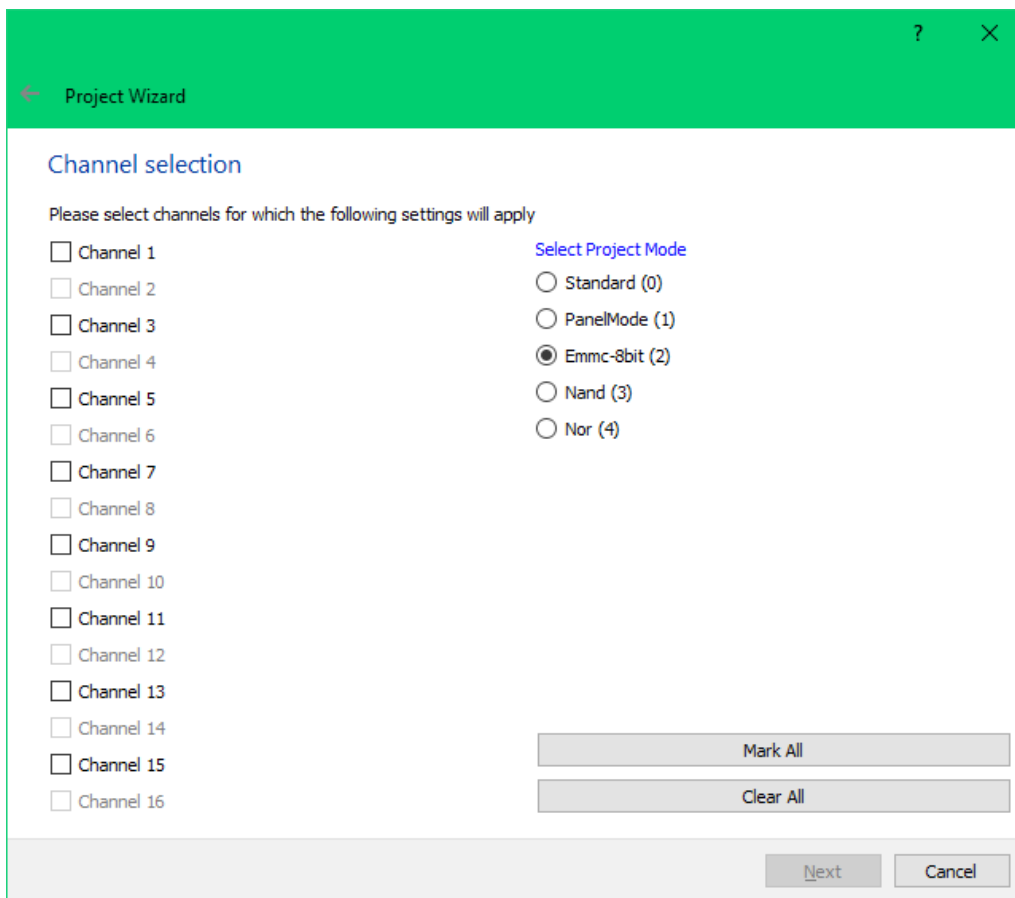
	MICRO	eMMC 1bit	eMMC 4bit	eMMC 8bit	NAND	NOR
MICRO	16	16	16			
EMMC 1bit	16	16	16			
EMMC 4bit	16	16	16			
EMMC 8bit				8		
NAND					4	
NOR						2

This means that you can program MICRO and eMMC using 1bit or 4bit, but you cannot program MICRO and NAND together. Once you select NAND memory for a channel, you can only program other NANDs with the remaining free channels. The same principle applies for eMMC 8bit and NOR memories.

Another consideration drives to the fact that a eMMC memory needs 2 ISP adjacent channels, a NAND memory 4 adjacent channels, a NOR memory 8 adjacent channels: this means, for example, that with a FLASHRUNNER2.0A16 you can program up to 2 NOR in parallel, while for a FLASHRUNNER2.0A08 you can program only one NOR memory.

2. Software Configuration

Project wizard of FlashRunner 2.0 Workbench could easily drive you to a working configuration.

If you selecting for example Emmc-8bit project mode will automatically disable channels on the left side of the project wizard page which will be reserved for connecting all the necessary data lines. Project wizard of FlashRunner 2.0 Workbench could easily drive you to a working configuration.

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Once you select the project mode, Project Wizard page will show you only device which are compatible with this modality: eMMC 1 and 4 data lines can be programmed in Standard and PanelMode. Once you get to the end of the Project Wizard, if you have a FlashRunner 2.0 connected, it will double check if FlashRunner 2.0 is set to the right operation mode and, if not, it will advise you if you want to change it to the right one or not.
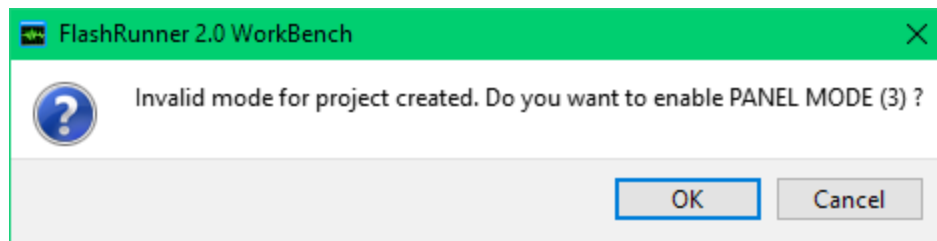
In any case, you can change it later on through FlashRunner 2.0 Workbench with the menu below.

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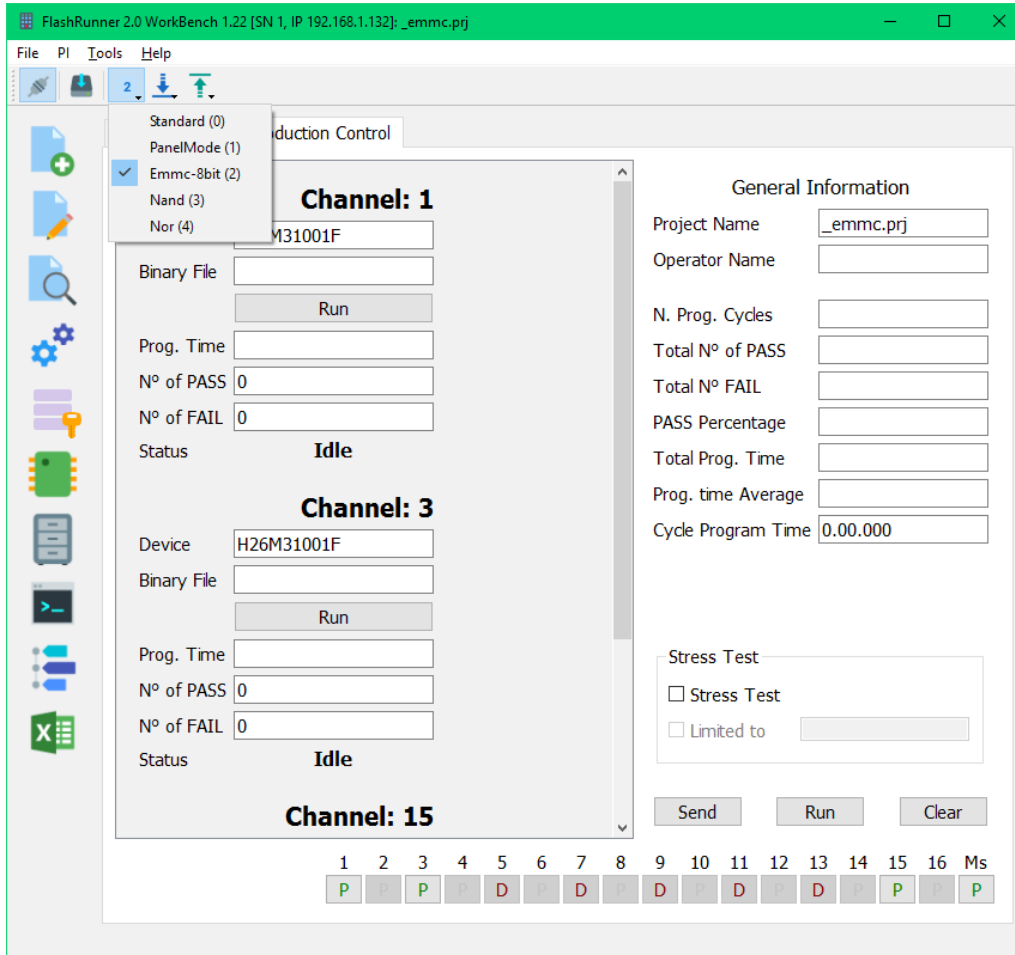
Alternatively, you can use the SETPANELMODE command (please refer to Programmer's Manual for more details):

- **SETPANELMODE 0**: standard mode, will program all devices, included eMMC 1bit and 4bit,

- **SETPANELMODE 1**: PanelMode will program all devices, included eMMC 1bit and 4bit, but you can't mix different protocols,

- **SETPANELMODE 2**: use this setting for eMMC 8bit

- **SETPANELMODE 3**: use this setting for NAND

- **SETPANELMODE 4**: use this setting for NOR

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3. Hardware configuration

PinMap tool, available on FlashRunner 2.0 Workbench is a comfortable tool which help users to do cable wirings. For configurations which requires more than one channel however you'll have to follow table below, which shows connections only the first channel and must be replicated for the following channels with the same schema:
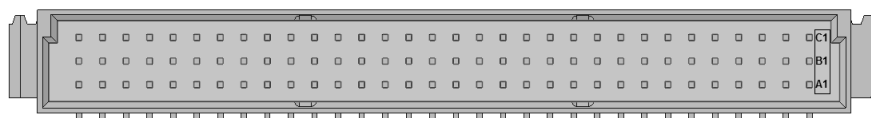
eMMC 1bit pinout:

Pin #	Pin name	Signal Name	Description
A1	1DIO0	RST	ISP Channel 1: Digital input/output 0
B1	1DIO1	CLK	ISP Channel 1: Digital input/output 1
C1	1DIO2	CMD	ISP Channel 1: Digital input/output 2
A2	1DIO3	DAT0	ISP Channel 1: Digital input/output 3

eMMC 4bit pinout:

Pin #	Pin name	Signal Name	Description
A1	1DIO0	RST	ISP Channel 1: Digital input/output 0
B1	1DIO1	CLK	ISP Channel 1: Digital input/output 1
C1	1DIO2	CMD	ISP Channel 1: Digital input/output 2
A2	1DIO3	DAT0	ISP Channel 1: Digital input/output 3
B2	1DIO4	DAT1	ISP Channel 1: Digital input/output 4
C2	1DIO5	DAT2	ISP Channel 1: Digital input/output 5
A3	1DIO6	DAT3	ISP Channel 1: Digital input/output 6

eMMC 8bit pinout:

Pin #	Pin name	Signal Name	Description
A1	1DIO0	RST	ISP Channel 1: Digital input/output 0
B1	1DIO1	CLK	ISP Channel 1: Digital input/output 1
C1	1DIO2	CMD	ISP Channel 1: Digital input/output 2
A2	1DIO3	DAT0	ISP Channel 1: Digital input/output 3
B2	1DIO4	DAT1	ISP Channel 1: Digital input/output 4
C2	1DIO5	DAT2	ISP Channel 1: Digital input/output 5
A3	1DIO6	DAT3	ISP Channel 1: Digital input/output 6

Pin #	Pin name	Signal Name	Description
C3	1DIO7	DAT4	ISP Channel 1: Digital input/output 7
A5	2DIO0	DAT5	ISP Channel 2: Digital input/output 0
B5	2DIO1	DAT6	ISP Channel 2: Digital input/output 1
C5	2DIO2	DAT7	ISP Channel 2: Digital input/output 2

NAND pinout:

Pin #	Pin name	Signal Name	Description
A1	1DIO0	CLE	ISP Channel 1: Digital input/output 0
B1	1DIO1	ALE	ISP Channel 1: Digital input/output 1
C1	1DIO2	CEn	ISP Channel 1: Digital input/output 2
A2	1DIO3	WEn	ISP Channel 1: Digital input/output 3
B2	1DIO4	REn	ISP Channel 1: Digital input/output 4
C2	1DIO5	WPn	ISP Channel 1: Digital input/output 5
A3	1DIO6	RBn	ISP Channel 1: Digital input/output 6
A5	2DIO0	IO0	ISP Channel 2: Digital input/output 0
B5	2DIO1	IO1	ISP Channel 2: Digital input/output 1
C5	2DIO2	IO2	ISP Channel 2: Digital input/output 2
A6	2DIO3	IO3	ISP Channel 2: Digital input/output 3
B6	2DIO4	IO4	ISP Channel 2: Digital input/output 4
C6	2DIO5	IO5	ISP Channel 2: Digital input/output 5
A7	2DIO6	IO6	ISP Channel 2: Digital input/output 6
C7	2DIO7	IO7	ISP Channel 2: Digital input/output 7
A9	3DIO0	IO8	ISP Channel 3: Digital input/output 0
B9	3DIO1	IO9	ISP Channel 3: Digital input/output 1
C9	3DIO2	IO10	ISP Channel 3: Digital input/output 2
A10	3DIO3	IO11	ISP Channel 3: Digital input/output 3
B10	3DIO4	IO12	ISP Channel 3: Digital input/output 4
C10	3DIO5	IO13	ISP Channel 3: Digital input/output 5
A11	3DIO6	IO14	ISP Channel 3: Digital input/output 6
C11	3DIO7	IO15	ISP Channel 3: Digital input/output 7

Next free channel will be channel 4, and the same signals schema will apply.

NOR pinout:

<coming soon>

4. Programming Times

The following table shows programming times for various memory types devices.

Device	Mem. Size	Conditions	Operations	Time
eMMC THGBM5G6A	64MB (portion)	25MHz	Program	4,2
eMMC THGBM5G6A	64MB (portion)	25MHz	Verify	4,2
NAND S34ML08G101	64MB (portion)	12,5 MHz	Program	15
NAND S34ML08G101	64MB (portion)	12,5 MHz	Program	13
NAND S34ML08G101	1GB	12,5 MHz	Blankcheck	128

Programming times depend on Programming Algorithm version, target board connections, communication mode, target microcontroller mask, and other conditions. Programming times for your actual system may therefore be different than the ones listed here. SMH Technologies reserves the right to modify Programming Algorithms at any time.

5. References

FlashRunner 2.0 User's Manual

FlashRunner 2.0 Programmer's Manual

Microcontroller-specific datasheets

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