SMH Technologies™
UNIVERSAL PRODUCTION IN-SYSTEM PROGRAMMING

SofTec™ Microsystems

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AN00155: Interfacing FlashRunner with Renesas V850E2 Devices

FlashRunner is a Universal In-System Programmer, which uses the principles of In-Circuit Programming to program Renesas V850E2 family microcontrollers. This Application Note describes how to properly set up and use FlashRunner to program V850E2 Flash devices.

This Application Note assumes that you are familiar with both FlashRunner and the main features of the V850E2 family. Full documentation about these topics is available in the FlashRunner user's manual and in device-specific datasheets.

1. Introduction

In-system programming of V850E2 microcontrollers is performed through 1-Wire UART serial protocol.

In order to use FlashRunner to perform in-system programming, you need to implement the appropriate in-circuit programming hardware interface on your application board.

Thanks to its in-system programming capabilities, FlashRunner allows you to program or update the content of the Flash memory when the chip is already plugged on the application board.

2. Hardware Configuration

The microcontroller's lines needed to program a V850E2 device are the following:

- **FLMD0:** Mode selection pin
- **FLMD1:** Mode selection pin
- **FLUR0RTX:** Digital bi-directional communication line
- **RESET:** Reset signal input pin. This LSI enters the reset state when this signal goes low.
- **VDD:** Device power supply voltage.
- **VSS:** Device power supply ground.

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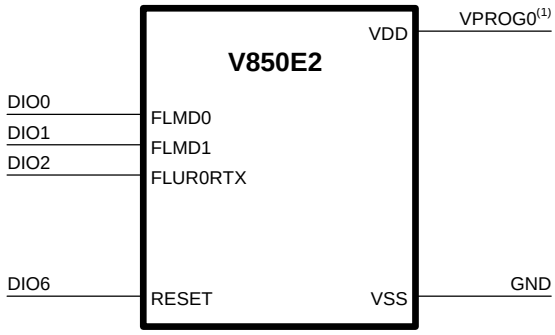
The lines mentioned above must be connected to the FlashRunner's "ISP" connector according to the following diagram:



(1) Connect this line if you want FlashRunner to automatically power the target device

3. Specific TCSETPAR Programming Commands

Overview

TCSETPAR commands set device-specific and programming algorithm-specific parameters. These commands must be sent after the **TCSETDEV** command and before a **TPSTART** / **TPEND** command block.

All of the following parameters must be correctly specified through the relative **TCSETPAR** commands (although the order with which these parameters are set is not important):

- VDD voltage;
- VDD_AUX voltage;
- Power Up time;
- Power Down time;
- Reset Up time;

- Reset Down time;
- Reset Drive mode;
- Clock oscillator frequency driven by FlashRunner;
- FOSC External oscillator frequency;
- Serial communication protocol;
- Communication BAUDRATE.

TCSETPAR VDD

Command syntax:

`TCSETPAR VDD <voltage mV>`

Parameters:

`voltage mV`: Target device supply voltage, expressed in millivolts.

Description:

This command is used to properly generate the voltage level of the ISP lines. Additionally, the specified voltage is routed to the VPROG0 line of the FlashRunner's "ISP" connector, which can be used as a supply voltage for the target board.

TPSETPAR VDD_AUX

Command syntax:

`TCSETPAR VDD_AUX <voltage mV>`

Parameters:

`voltage mV`: Auxiliary supply voltage, expressed in millivolts, in the range 3000-14500mV.

Description:

This command is used to generate an optional, auxiliary voltage level for user purposes. The specified voltage is routed to the VPROG1 line of the FlashRunner "ISP" connector.

A value of 0 drives the VPROG1 line to GND. If the **`TCSETPAR VDD_AUX`** is not sent, the VPROG1 line is driven to HiZ.

TCSETPAR PWUP

Command syntax:

`TCSETPAR PWUP <time ms>`

Parameters:

`time ms`: Power rising time, expressed in milliseconds.

Description:

This command is necessary because, to enter the programming mode, FlashRunner must properly drive the V_{DD} line during the power-on reset.

The V_{DD} rising time (PWUP) is expressed in milliseconds and depends on the features of your target board. Make sure to choose a value large enough to ensure that the V_{DD} signal reaches the high logic level within the specified time. Note that, if the V_{DD} line has a high load, a longer time is required for the V_{DD} signal to reach the high logic level. If PWUP is not long enough, FlashRunner could not be able to enter the programming mode.

TCSETPAR PWDOWN

Command syntax:

`TCSETPAR PWDOWN <time ms>`

Parameters:

`time ms`: Power falling time, expressed in milliseconds.

Description:

The V_{DD} falling time (PWDOWN) is expressed in milliseconds and depends on the features of your target board. Make sure to choose a value large enough to ensure that the V_{DD} signal reaches the low logic level within the specified time. Note that, if the V_{DD} line has a high load, a longer time is required for the V_{DD} signal to reach the low logic level.

TCSETPAR RSTUP

Command syntax:

`TCSETPAR RSTUP <time µs>`

Parameters:

`time µs`: Reset rising time, expressed in microseconds.

Description:

The Reset rising time (RSTUP) is expressed in microseconds and depends on the features of your target board. Make sure to choose a value large enough to ensure that the Reset signal reaches the high logic level within the specified time. Note that, if the Reset line has a high load, a longer time is required for the Reset signal to reach the high logic level. If RSTUP isn't long enough, FlashRunner could not be able to enter the JTAG programming mode.

TCSETPAR RSTDOWN

Command syntax:

`TCSETPAR RSTDOWN <time µs>`

Parameters:

`time µs`: Reset falling time, expressed in microseconds.

Description:

The Reset falling time (RSTDOWN) is expressed in microseconds and depends on the features of your target board. Make sure to choose a value large enough to ensure that the Reset signal reaches the low logic level within the specified time. Note that, if the Reset line has a high load, a longer time is required for the Reset signal to reach the low logic level.

TCSETPAR RSTDRV

Command syntax:

`TCSETPAR RSTDRV <mode>`

Parameters:

`mode`: Reset drive mode.

Description:

The Reset Drive Mode can be OPENDRAIN or PUSHPULL.

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TCSETPAR CLKOUT

Command syntax:

`TCSETPAR CLKOUT 25000000 | 12500000 | 6250000 | 0`

Command options:

Frequency of a clock signal to be generated at the CLOCKOUT pin of the FlashRunner “ISP” connector, expressed in Hertz.

Description:

Generates an auxiliary clock signal at the CLOCKOUT pin of the FlashRunner “ISP” connector. This signal can be used to enter the target device’s UART mode when the target device does not have an external clock. Furthermore, this signal can be used to speed up programming (when you want to use a clock faster than that provided by your target board).

Make sure that the clock frequency you select isn’t greater than the maximum allowed frequency for your device. If the target device has an internal frequency divider, the actual device’s frequency will be a fraction of the CLKOUT frequency.

If you specify **`0`** as the CLKOUT frequency, no clock signal is generated.

TCSETPAR FOSC

Command syntax:

`TCSETPAR FOSC <frequency Hz>`

Parameters:

`frequency Hz`: External oscillator frequency, expressed in Hertz.

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Description:

This command is used to set up the frequency of the external oscillator mounted on the target board.

TCSETPAR CMODE

Command syntax:

`TCSETPAR CMODE <mode>`

Parameters:

`mode`: Serial protocol to use.

Description:

Select the protocol to use for communication with the LSI. Possibile value:

UART: 1-Wire asynchronous serial comunication.

TCSETPAR BAUDRATE

Command syntax:

`TCSETPAR BAUDRATE <value>`

Parameters:

`value`: value of serial interface baudrate.

Description:

This command is used to set up the serial baudrate. Possible values are 9600, 115200, 500000.

4. Specific TPCMD Programming Commands

Overview

TPCMD commands perform a programming operation (i.e. mass erase, program, verify, etc.) These command must be sent within a **TPSTART** / **TPEND** command block.

Renesas V850E2 -specific target programming commands are the following:

- **TPCMD MASSERASE**;
- **TPCMD BLOCKERASE**;
- **TPCMD BLANKCHECK**;
- **TPCMD PROGRAM**;
- **TPCMD VERIFY**;
- **TPCMD PROTECT**;
- **TPCMD READ**;
- **TPCMD RUN**.

TPCMD MASSERASE

Command syntax:

TPCMD MASSERASE C|F|E

Command options:

C|F|E: Specifies that this command refer to the whole device memory(**C**), Flash memory (**F**) or to the EEPROM memory (**E**).

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Description:

It erases all the device (**C**), Flash memory (**F**) or EEPROM memory (**E**).

TPCMD BLOCKERASE

Command syntax:

`TPCMD ERASE F|E <tgt start addr> <len>`

Command options:

`F|E:`	Specifies that this command refer to the Flash memory (**F**) or to the EEPROM memory (**E**).
`tgt start address`:	Device memory location from where the block erase operation will start.
`len`:	Number of locations to be block erased.

Description:

It erases blocks of locations in the Flash memory (**F**) or in the EEPROM memory (**E**). **`tgt start address`** is the start address of a block. **`len`** is such as the final address of the range to be erased is exactly the final address of a memory block. The start address is the logical address specified in each single device datasheet or User's Guide under "Memory" chapter.

TPCMD BLANKCHECK

Command syntax:

`TPCMD BLANKCHECK F|E <tgt start addr> <len>`

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Command parameters and options:

F|E:	Specifies Flash (**F**) memory or EEPROM (**E**) memory.
tgt start address:	Device memory location from where the blankcheck operation will start.
len:	Number of locations to be blankchecked.

Description:

It blankchecks Flash memory or EEPROM memory. Blankchecks **len** locations starting from the address specified by **tgt start address**. The start address is the logical address specified in each single device datasheet or User's Guide under "Memory" chapter.

TPCMD PROGRAM

Command syntax:

```
TPCMD PROGRAM F|E|O|D <src offset> <tgt start addr> <len> ID_TAG
```

Command parameters and options:

F|E|O|D:	Specifies Flash (**F**) memory, EEPROM (**E**) memory, Option Bytes (**O**) or OnChipDebug ID (**D**).
src offset:	Offset from the beginning of the source memory.
tgt start addr:	Device memory location from where the program operation will start.
len:	Number of locations to be programmed.
ID_TAG:	Required only for EEPROM memory, if present the source binary already have the ID TAG inside, otherwise FlashRunner add it before sending the data to LSI.

Description:

It programs **len** locations of Flash memory or EEPROM memory starting from the **tgt start addr** address.

len specifies the number of locations to be programmed. **tgt start addr** is the logical address specified in each single device datasheet or User's Guide under "Memory" chapter.

For Option Bytes the length must be $24.

For OnChipDebug ID the length must be $C.

TPCMD VERIFY

Command syntax:

TPCMD VERIFY F|E R <src offset> <tgt start addr> <len>

Command parameters and options:

F|E:	Specifies Flash (**F**) memory or EEPROM (**E**) memory.
R	Specifies Readout (**R**).
src offset:	Offset from the beginning of the source memory.
tgt start addr:	Device memory location from where the verify operation will start.
len:	Number of locations to be verified

Description:

It verifies **len** locations of Flash memory or EEPROM memory starting from the **tgt start addr** address. **len** specifies the number of locations to be verified.

TPCMD PROTECT

Command syntax:

TPCMD PROTECT F <security flag> <Boot block cluster block number> <FSW start block> <FSW end block>

Command parameters and options:

F: Specifies Flash (**F**) memory.

Boot block cluster block number Specifies which is the Boot block cluster number (See target User Manual for detailed description)

Security flags

Security Flags:

```
bit7: "1" fixed value
bit6: "1" fixed value
bit5: 0->Read disable
      1->Read Enable
bit4: 0->Write disable
      1->Write Enable
bit3: 0->Chip Erase disable
      1-> Chip Erase Enable
bit2: 0->Block Erase disable
      1->Block Erase Enable
bit1: 0->Boot cluster protected
      1->Boot cluster Rewritable
bit0: "1" fixed value.
```

FSW start block: FSW start block number.

FSW end block: FSW end block number.

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Description:

It specifies which is the “Boot block cluster number” and sets the security flags for a contiguous set of blocks. This set is specified with **`FSW start block`** and **`FSW end block`** which define respectively the first block and the last block for which the **`Security flag`** will apply. Each bit of **`Security flag`** defines a specific restriction in the FSW, so please be careful defining each single byte of the **`Security flag`** byte. Each block size is defined by user firmware. Once a flag is disabled could be reactivate only by means of MASSERASE C command except for Chip Erase and Block Erase bit flag, which could not be changed.

TPCMD READ

Command syntax:

`TPCMD READ F|E|S|O|D <tgt start addr> <len>`

`TPCMD READ IDCODE`

Command parameters and options:

`F|E|S|O|D`:	Specifies Flash (**F**) memory, EEPROM (**E**) memory, Signature (**S**), Option Bytes (**O**) or OnChipDebug ID (**D**).
`tgt start addr`:	Device memory location from where the read operation will start.
`len`:	Number of locations to be read.

Description:

It reads **`len`** locations of Flash memory or EEPROM memory starting from the **`tgt start addr`** address. **`len`** specifies the number of locations to be read.

For Signature(S) , Option Bytes(O) and OnChipDebug ID(D) tgt start addr and len shoud be set to 0.

If O is selected, the programming algorithms reads some information about the device.

TPCMD RUN

Command syntax:

`TPCMD RUN`

Command parameters:

None.

Description:

It runs the target application.

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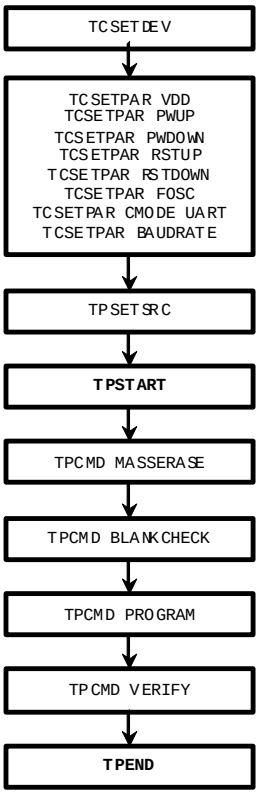
5. Typical Programming Flow

The following flow chart illustrates typical steps to help you write your own script file.



6. Script Example

The example below shows a typical programming flow for a Renesas V850E2 device.

```
;
; FLASHRUNNER SCRIPT EXAMPLE FOR NEC UPD70F4006
;
; Use this example as a starting point for your specific programming needs
;
; ----------
;
; Hardware connections for UART protocol
; DIO0 (FLMD0)
; DIO1 (FLMD1)
; DIO2 (TxD/RxD) Digital bi-directional line
; DIO6 (RESET)
;
; Turns off logging
#LOG_OFF
; Halt on errors
#HALT_ON FAIL

; Sets device
TCSETDEV NEC UPD70F4006 V850_B

;------------------------
;FLASHRUNNER I/O Settings
;------------------------

; Target voltage, mV (change as needed)
TCSETPAR VDD 4200

; Clock oscillator frequency driven by FlashRunner, Hz
; Possible frequencies are: 25000000 divided by a 16-bit prescaler, 0 (DISABLED)
TCSETPAR CLKOUT 0

; VDD rise-time, ms (from 0 ms to 65535 ms)
TCSETPAR PWUP 10

; VDD fall-time, ms (from 0 ms to 65535 ms)
TCSETPAR PWDOWN 10

; RESET rise-time, us (from 0 us to 65535 us)
```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```
TCSETPAR RSTUP 100

; RESET fall-time, us (from 0 us to 65535 us)
TCSETPAR RSTDOWN 100

; RESET drive mode: OPENDRAIN or PUSHPULL
TCSETPAR RSTDRV OPENDRAIN

;--------------------
;V850_B ALGO Settings
;--------------------
TCSETPAR CMODE UART

; External clock source frequency, Hz (change as needed)
; For this device the maximum FOSC is 80000000 Hz
TCSETPAR FOSC 80000000

; Baudrate settings, bps (change as needed)
; Only the UART communication mode need to set the baudrate.
; FlashRunner ignores the Baudrate TCSETPAR command if it is transmitted in modes other than the UART communication mode.
; For this device the possible values are 9600, 115200, 500000 bps.
TCSETPAR BAUDRATE 500000

;---------------------------
;Start Programming operation
;---------------------------

; Image file to be programmed (must be placed in the \BINARIES directory)
TPSETSRC FILE TEST.FRB

; Starts programming block
TPSTART

;--------------
;FLASH commands
;--------------

;MASSERASE operation has the following options:
;C: Mass erases whole memory
;F: Mass erases FLASH memory
;E: Mass erases EEPROM memory
TPCMD MASSERASE C

; Blank checks Flash memory (change address and length as needed)
```

```
TPCMD BLANKCHECK F $0 $180000

; Programs Flash memory (change addresses and length as needed)
TPCMD PROGRAM F $0 $0 $180000

; Verifies Flash memory (change addresses and length as needed)
TPCMD VERIFY F R $0 $0 $180000

;--------------
;EEPROM commands
;--------------

; Blank checks EEPROM memory (change address and length as needed)
TPCMD BLANKCHECK E $2000000 $10000

; Programs EEPROM memory (change addresses and length as needed)
TPCMD PROGRAM E $2000000 $2000000 $10000 BLOCK ID_TAG

; Verifies EEPROM memory (change addresses and length as needed)
TPCMD VERIFY E R $2000000 $2000000 $10000 ID_TAG

; Ends programming block
TPEND
```

The FlashRunner's system software setup will install script examples specific for each device of the V850E2 family on your PC.

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7. Programming Times

The following table shows programming times for selected Renesas V850E2 devices.

Device	Mem. Size	Conditions	Operations	Time
uPD70F4006	1536KB Flash + 64KB EEPROM	FR01LAN, BAUDRATE= 500 KHz	Erase + Blankcheck + Program + Verify	141.28 s
uPD70F4006	1536KB Flash + 64KB EEPROM	FR04A08, BAUDRATE= 500 KHz	Erase + Blankcheck + Program + Verify	147.20 s

Programming times depend on Programming Algorithm version, target board connections, communication mode, target microcontroller mask, and other conditions. Programming times for your actual system may therefore be different than the ones listed here. SMH Technologies reserves the right to modify Programming Algorithms at any time.

8. References

FlashRunner User's Manual.

Microcontroller-specific Datasheets and User's Guides.