SMH Technologies
UNIVERSAL PRODUCTION
IN–SYSTEM PROGRAMMING

27/09/2012 Samuele Stefanoni

DC10502

AN00150: Interfacing FlashRunner with Atmel ATXMEGA Devices

FlashRunner is a Universal In-System Programmer, which uses the principles of In-Circuit Programming to program Atmel ATXMEGA family microcontrollers.

This Application Note assumes that you are familiar with both FlashRunner and the main features of the ATXMEGA family. Full documentation about these topics is available in the FlashRunner user's manual and in device-specific datasheets.

1. Introduction

In-system programming of ATXMEGA microcontrollers is performed through JTAG IEEE 1149.1 standard protocol or through PDI protocol. Please check on your device script file which protocols are implemented.

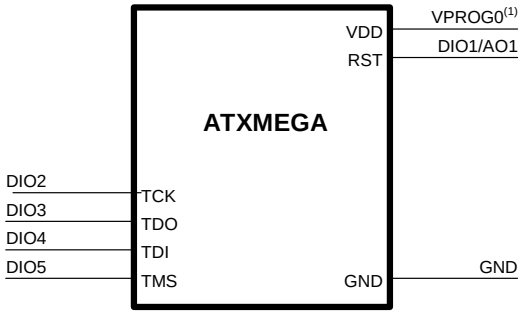
In order to use FlashRunner to perform in-system programming, you need to implement the appropriate in-circuit programming hardware interface on your application board.

2. Hardware Configuration

The microcontroller lines needed to program an ATXMEGA device through JTAG protocol are the following:

- **TMS:** Test mode select.
- **TCK:** Test Clock.
- **TDI:** Test Data In.
- **TDO:** Test Data Out
- **RST:** Device reset input/output pin.
- **VDD:** Device power supply voltage.
- **GND:** Device power supply ground.

The lines mentioned above must be connected to the FlashRunner's "ISP" connector according to the following diagram:

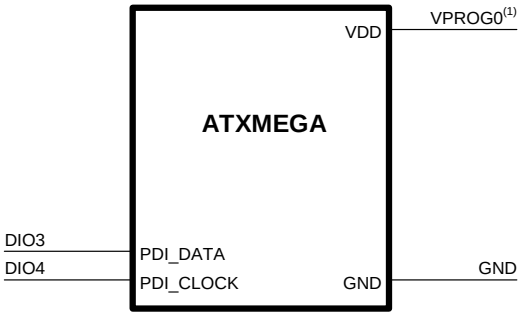


(1) Connect this line if you want FlashRunner to automatically power the target device

The microcontroller lines needed to program an ATXMEGA device through PDI protocol are the following:

- **PDI_DATA:** Digital input/output line
- **PDI_CLK:** Output digital line.
- **VDD:** Device power supply voltage.
- **GND:** Device power supply ground.

The lines mentioned above must be connected to the FlashRunner's "ISP" connector according to the following diagram:



(1) Connect this line if you want FlashRunner to automatically power the target device

3. Specific TCSETPAR Programming Commands

Overview

TCSETPAR commands set device-specific and programming algorithm-specific parameters. These commands must be sent after the **TCSETDEV** command and before a **TPSTART** / **TPEND** command block.

All of the following parameters must be correctly specified through the relative **TCSETPAR** commands (although the order with which these parameters are set is not important):

- Communication frequency;
- Communication mode.

TCSETPAR CLK

Command syntax:

TCSETPAR CLK <frequency Hz>

Parameters:

frequency Hz: communication frequency, expressed in Hertz.

Description:

This command is used to set up the communication frequency between FlashRunner and target microcontroller. Must be less that 12,5 Mhz.

TCSETPAR CMODE

Command syntax:

TCSETPAR CMODE <communication protocol>

Parameters:

communication protocol: **"JTAG"** or **"PDI"**.

Description:

Specifies the communication protocol used between FlashRunner and target microcontroller.

4. Specific TPCMD Programming Commands

Overview

TPCMD commands perform a programming operation (i.e. mass erase, program, verify, etc.) These command must be sent within a **TPSTART** / **TPEND** command block.

Atmel ATXMEGA-specific target programming commands are the following:

- **TPCMD BLANKCHECK**;
- **TPCMD MASSERASE**;
- **TPCMD PROGRAM**;
- **TPCMD VERIFY**;
- **TPCMD READ**;
- **TPCMD RUN**.

TPCMD BLANKCHECK

Command syntax:

TPCMD BLANKCHECK F|E <tgt start addr> <len>

Command parameters and options:

F|E:	Specifies Flash (**F**) or EEPROM (**E**) memory.
tgt start address:	Device memory location from where the blankcheck operation will start.
len:	Number of locations to be blankchecked.

Description:

Blankchecks Flash or EEPROM memory. Blankchecks **len** locations starting from the address specified by **tgt start address**. The start address is not related to PDI memory map but is the logical address specified in each single device datasheet under “Memory” chapter.

Flash memory is organized as 16-bit locations: **len** specifies the number of 16-bit words to be blankchecked.

EEPROM memory is organized as 8-bit locations: **len** specifies the number of bytes to be blankchecked.

TPCMD MASSERASE

Command syntax:

TPCMD MASSERASE C|F|U

Command options:

C|F|U:	Specifies Chip (**C**), Flash (**F**) memory or User Signature (**U**)

Description:

‘C’ parameter mass erases Flash memory, EEPROM memory and user signature. Fuse bits are not erased. **‘F’** mass erases Flash memory, **‘U’** mass erase user signature. Be aware that **MASSERASE C** command automatically set **EESAVE** bit of **FUSEBYTE5** to 1, instead **MASSERASE F** command automatically set **EESAVE** bit of **FUSEBYTE5** to 0.

TPCMD PROGRAM

Command syntax:

`TPCMD PROGRAM F|E|U|L <src offset> <tgt start addr> <len>`

Command parameters and options:

`F|E|U|L`:	Specifies Flash (**F**), EEPROM (**E**) memory, User signature (**U**) or Fuses and Locks (**L**).
`src offset`:	Offset from the beginning of the source memory.
`tgt start addr`:	Device memory location from where the program operation will start.
`len`:	Number of locations to be programmed.

Description:

Programs **`len`** locations of Flash or EEPROM memory starting from the **`tgt start addr`** address, or program the specified Fuse Bits or Lock Bits.

Flash memory is organized as 16-bit locations: **`len`** specifies the number of 16-bit words to be programmed. **`tgt start addr`** is not related to PDI memory map but is the logical address specified in each single device datasheet under “Memory” chapter.

EEPROM memory is organized as 8-bit locations: len specifies the number of bytes to be programmed**. `tgt start addr`** is not related to PDI memory map but is the logical address specified in each single device datasheet under “Memory” chapter.

User Signature is organized as 16-bit locations: **`len`** specifies the number of 16-bit words to be programmed. **`tgt start addr`** start from $0 and FlashRunner will add runtime the correct offset.

Fuses and Lock registers are organized as 8-bit locations: **`len`** specifies the number of bytes to be programmed. **`tgt start addr`** start from $0 and FlashRunner will add runtime the correct offset.

TPCMD VERIFY

Command syntax:

```
TPCMD VERIFY F|E R|C <src offset> <tgt start addr>
                    <len>
```

Command parameters and options:

F|E:	Specifies Flash (**F**) or EEPROM (**E**) memory.
R|S	Specifies Readout (**R**) or CRC (S).
src offset:	Offset from the beginning of the source memory.
tgt start addr:	Device memory location from where the verify operation will start.
len:	Number of locations to be verified

Description:

Verifies **len** locations of Flash or EEPROM memory starting from the **tgt start addr** address. The CRC parameter print back the CRC of the entire flash memory calculated from target microcontroller.

Flash memory is organized as 16-bit locations: **len** specifies the number of 16-bit words to be verified.

EEPROM memory is organized as 8-bit locations: **len** specifies the number of bytes to be verified.

TPCMD READ

Command syntax:

```
TPCMD READ F|E|C|L|U <tgt start addr> <len>
```

Command parameters and options:

F|E|C|L|U:	Specifies Flash (**F**), EEPROM (**E**) memory, Calibration Row (**C**), Fuses and Locks (**L**), User Signature (**U**).
tgt start addr:	Device memory location from where the read operation will start.
len:	Number of locations to be read.

Description:

Reads len locations of Flash or EEPROM memory starting from the tgt start addr address, or reads the specified Fuse Bits or Lock Bits.

Flash memory is organized as 16-bit locations: **`len`** specifies the number of 16-bit words to be programmed. **`tgt start addr`** is not related to PDI memory map but is the logical address specified in each single device datasheet under “Memory” chapter.

EEPROM memory is organized as 8-bit locations: **`len`** specifies the number of bytes to be programmed. **`tgt start addr`** is not related to PDI memory map but is the logical address specified in each single device datasheet under “Memory” chapter.

User Signature is organized as 16-bit locations: **`len`** specifies the number of 16-bit words to be programmed. **`tgt start addr`** start from $0 and FlashRunner will add runtime the correct offset.

Calibration Row, Fuses and lock registers are organized as 8-bit locations: **`len`** specifies the number of bytes to be programmed. **`tgt start addr`** start from $0 and FlashRunner will add runtime the correct offset.

TPCMD RUN

Command syntax:

`TPCMD RUN`

Command parameters:

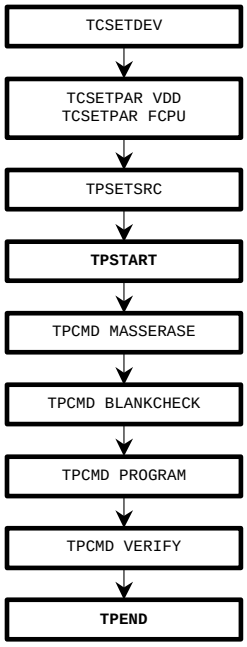
None.

Description:

Runs the target application.

5. Typical Programming Flow

The following flow chart illustrates typical steps to help you write your own script file.



6. Script Example

The example below shows a typical programming flow for an Atmel ATXMEGA64A3 device.

```
;
; FLASHRUNNER SCRIPT EXAMPLE FOR ATMEL ATXMEGA64A;
; Use this example as a starting point for your specific programming needs
;
; ----------
;
; Hardware connections
;
; DIO1/AO1    (NRST)
; DIO2        (JTCK)
; DIO3        (JTDO)
; DIO4        (JTDI)
; DIO5        (JTMS)
;
; Turns off logging
#LOG_OFF
; Halt on errors
#HALT_ON FAIL

; Sets device
TCSETDEV ATMEL ATXMEGA64A3 ATXMEGA

; ------------------------------------------------------------------------------------------------------------
; ATTENTION: for more information on the available commands and parameter tuning
; please visit our website: http:\www.smh-tech.com, click on 'Support & download' menu, Download Area section and
; 'Application Note' subsection and download the document related to the specific programming algorithm
; ------------------------------------------------------------------------------------------------------------

;-------------------------
; FLASHRUNNER I/O Settings
;-------------------------

; Target voltage, mV (change as needed)
TCSETPAR VDD 2600
; VPROG1 voltage, mV (from 3000 to 14500, 0 to disable)(change as needed)
; TCSETPAR VDD_AUX 3000
; Clock oscillator frequency driven by FlashRunner, Hz
; Possible frequencies are: 25000000, 12500000, 6250000, 0 (DISABLED)
```

```
TCSETPAR CLKOUT 0
; RESET down time (from 0 us to 65535 us)
TCSETPAR RSTDOWN 1000
; RESET up time (from 0 us to 65535 us)
TCSETPAR RSTUP 1000
; RESET driving mode (PUSHPULL or OPENDRAIN)
TCSETPAR RSTDRV OPENDRAIN
; Power down time (from 0 ms to 65535 ms)
TCSETPAR PWDOWN 10
; Power up time (from 0 ms to 65535 ms)
TCSETPAR PWUP 10

;----------------------
; ATXMEGA ALGO Settings
;----------------------

; Set the frequency of the JTAG channel, Hz (change as needed)
; It must be less then 12500000 frequency
TCSETPAR JTCLK 500000

; Set the comunication protocol
; ATTENTION: only JTAG available in this version
TCSETPAR CMODE JTAG

;---------------------------
; Start Programming operation
;---------------------------

; Image file to be programmed (must be placed in the \BINARIES directory)
TPSETSRC FILE FLASH.FRB
; Starts programming block
TPSTART

;---------------
; FLASH commands
;---------------

; Mass erases Chip
; ATTENTION: this commnad automatically set EESAVE bit of FUSEBYTE5 to 1
TPCMD MASSERASE C
; Blank checks Flash memory (change address and length as needed)
TPCMD BLANKCHECK F $0 $8800
; Blank checks EEPROM memory (change address and length as needed)
TPCMD BLANKCHECK E $1000 $800
; Programs Flash memory (change source, target address and length as needed)
```

```
TPCMD PROGRAM F $0 $0 $8800
; Programs EEPROM memory (change source, target address and length as needed)
TPCMD PROGRAM E $0 $1000 $800
; Verifies Flash memory (change source, target address and length as needed)
; If you want you can choose beetween two type of verify:
; 1) Read-Out method ®. Slow but secure
; 2) CheckSum method (S). Fast but not secure
TPCMD VERIFY F R $0 $0 $8800

; Verifies EEPROM memory (change source, target address and length as needed)
TPCMD VERIFY E R $0 $1000 $800
; Ends programming block
TPEND
```

The FlashRunner's system software setup will install script examples specific for each device of the ATXMEGA family on your PC.

7. Programming Times

The following table shows programming times for selected Atmel ATXMEGA family devices.

Device	Mem. Size	Conditions	Operations	Time
ATMEGA64A3	68 Kb F + 2 Kb E	6,25 Mhz JTAG	Erase + Program + Verify	13,26 s

Programming times depend on Programming Algorithm version, target board connections, communication mode, target microcontroller mask, and other conditions. Programming times for your actual system may therefore be different than the ones listed here. SMH Technologies reserves the right to modify Programming Algorithms at any time.

8. References

FlashRunner user's manual

Microcontroller-specific datasheets